

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 1. (Currently Amended) A method of exporting from a data
2 processor emulation information including emulation control
3 information and emulation data, comprising:

4 arranging the emulation information into fixed length
5 information blocks;

6 outputting a sequence of the information blocks from the
7 data processor via a plurality of terminals of the data processor;
8 and

9 said arranging step including providing some of the
10 information blocks of the sequence with relative proportions of
11 emulation control information and emulation data that differ from
12 the relative proportions of emulation control information and
13 emulation data in other blocks of the sequence;

14 storing comparison data;

15 comparing respective sections of emulation data with the
16 stored comparison data; and

17 wherein the emulation control information in one of the
18 information blocks includes a compression map indicative of whether
19 the sections of the emulation data match the stored comparison
20 data.

2 to 4. (Canceled)

1 5. (Currently Amended) The A method of Claim 1, wherein
2 exporting from a data processor emulation information including
3 emulation control information and emulation data, comprising:

4 arranging the emulation information into fixed length
5 information blocks, the emulation data in one of the information

6 blocks includes bits indicating whether the data processor
7 performed data processing operations during a corresponding clock
8 cycle;

9 outputting a sequence of the information blocks from the
10 data processor via a plurality of terminals of the data processor;
11 and

12 said arranging step including providing some of the
13 information blocks of the sequence with relative proportions of
14 emulation control information and emulation data that differ from
15 the relative proportions of emulation control information and
16 emulation data in other blocks of the sequence.

6 to 12. (Canceled)

1 13. (Currently Amended) An integrated circuit device,
2 comprising:

3 a data processing portion for performing data processing
4 operations;

5 an emulation information collector coupled to said data
6 processing portion for receiving emulation data therefrom, said
7 collector operable for arranging the emulation data and associated
8 emulation control information into fixed length information blocks;

9 a plurality of terminals coupled to said collector for
10 permitting said collector to communicate with an emulation
11 controller located externally of said integrated circuit device;
12 and

13 said collector operable for providing to said terminals a
14 sequence of said information blocks to be output to the emulation
15 controller, said collector further operable for providing some of
16 the information blocks of the sequence with relative proportions of
17 emulation control information and emulation data that differ from

18 the relative proportions of emulation control information and
19 emulation data in other blocks of the sequence;
20 a comparison data register storing comparison data;
21 a comparitor connected to said comparison data register and
22 receiving emulation data generating an indication of a match
23 between corresponding sections of said comparison data and said
24 emulation data; and
25 wherein the emulation control information in one of the
26 information blocks includes a compression map indicative of whether
27 the sections of the emulation data match the stored comparison
28 data.

14 to 16. (Canceled)

1 17. (Currently Amended) The An integrated circuit device of
2 ~~Claim 13, wherein comprising:~~
3 a data processing portion for performing data processing
4 operations;
5 an emulation information collector coupled to said data
6 processing portion for receiving emulation data therefrom, said
7 collector operable for arranging the emulation data and associated
8 emulation control information into fixed length information blocks,
9 the emulation data in one of the information blocks includes bits
10 indicating whether the data processor performed data processing
11 operations during a corresponding clock cycle;
12 a plurality of terminals coupled to said collector for
13 permitting said collector to communicate with an emulation
14 controller located externally of said integrated circuit device;
15 and
16 said collector operable for providing to said terminals a
17 sequence of said information blocks to be output to the emulation
18 controller, said collector further operable for providing some of

19 the information blocks of the sequence with relative proportions of
20 emulation control information and emulation data that differ from
21 the relative proportions of emulation control information and
22 emulation data in other blocks of the sequence.

18 to 27. (Canceled)